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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1   1.   (currently amended) A method of caching free cell pointers pointing to
2   memory buffers configured to store data traffic of network connections, the method comprising:
3   storing free cell pointers into a pointer random access memory (RAM), wherein
4   each free cell pointer points to a memory buffer that is vacant and available for storing data
5   traffic;
6   temporarily storing at least one free cell pointer from the pointer RAM into
7   internal cache configured to assist in lowering a frequency of reads from and writes to the pointer
8   RAM;
9   receiving a request from an external integrated circuit for one or more free cell
10   pointers;
11   sending one or more free cell pointers to one or more queues of the external
12   integrated circuit, the one or more free cell pointers including the at least one free cell pointer
13   temporarily stored in the internal cache, wherein each free cell pointer in the one or more free
14   cell pointers in a the one or more queues queue is configured to become a write cell pointer;
15   receiving at least one write cell pointer and a corresponding cell descriptor from
16   the external integrated circuit; and
17   calculating free cell pointer counter values in order to keep track of the free cell
18   pointers.

1   2.   (original) The method of Claim 1, wherein the pointer random access
2   memory (RAM) is external to controller circuitry configured to control the steps of the method.

1   3.   (original) The method of Claim 1, wherein the external integrated circuit
2   is an egress backplane interface subsystem (EBISS), and the queues of the external integrated
3   circuit are first in, first out (FIFO) queues.

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1   4.   (original) The method of Claim 1, further comprising sending read cell

2 pointers with corresponding cell descriptors to the external integrated circuit, wherein each read

3 cell pointer points to a memory buffer that has been read and that is free to be reused.

1   5.   (original) The method of Claim 1, wherein the step of storing free cell

2 pointers comprises:

3   storing odd free cell pointers in an odd free list of the pointer RAM; and

4   storing even free cell pointers in an even free list of the pointer RAM.

1   6.   (original) The method of Claim 1, wherein the step of temporarily storing

2 free cell pointers comprises:

3   storing odd free cell pointers in an odd free space of internal cache; and

4   storing even free cell pointers in an even free space of internal cache.

1   7.   (original) The method of Claim 4, wherein the step of calculating free

2 counter values comprises performing at least one of:

3   incrementing a free counter value to account for a cell pointer that has been sent

4 to the pointer RAM; and

5   decrementing a free counter value to account for a cell pointer that has been

6 received from the pointer RAM.

1   8.   (original) The method of Claim 1, wherein the step of calculating free

2 counter values comprises determining that a free counter value of internal cache is above a high

3 threshold, and wherein the method further comprises writing a block of cell pointers in a burst to

4 the pointer RAM.

1   9.   (original) The method of Claim 1, wherein the step of calculating free

2 counter values comprises determining that a free counter value of internal cache is below a low

3 threshold, and wherein the method further comprises reading a block of free cell pointers in a

4 burst from the pointer RAM.

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1   10.   (original) The method of Claim 1, wherein the step of calculating free

2   counter values comprises determining that a free counter value of internal cache is above an

3   overload threshold, and wherein the method further comprises temporarily blocking storing of

4   additional free cell pointers into internal cache.

1   11.   (currently amended) An integrated circuit configured to cache free cell

2   pointers pointing to memory buffers configured to store data traffic of network connections, the

3   integrated circuit comprising:

4   controller circuitry configured to control operations of:

5   storing free cell pointers into a pointer random access memory (RAM), wherein

6   each free cell pointer points to a memory buffer that is vacant and available for storing data

7   traffic;

8   temporarily storing at least one free cell pointer <u>from the pointer RAM</u> into

9   internal cache configured to assist in lowering a frequency of reads from and writes to the pointer

10   RAM;

11   receiving a request from an external integrated circuit for free cell pointers;

12   sending <u>one or more</u> free cell pointers to <u>one or more</u> queues of the external

13   integrated circuit, <u>wherein the one or more free cell pointers comprise the at least one free cell</u>

14   <u>pointer temporarily stored in the internal cache,</u> wherein each free cell pointer <u>in the one or more</u>

15   <u>free cell pointers in a</u> <s>a</s><u>the one or more queues</u> <s>queue</s> is configured to become a write cell pointer;

16   receiving at least one write cell pointer and a corresponding cell descriptor from

17   the external integrated circuit; and

18   calculating free cell pointer counter values in order to keep track of the free cell

19   pointers.

1   12.   (original) The integrated circuit of Claim 11, wherein the pointer random

2   access memory (RAM) is external to controller circuitry.

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1   13.   (original) The integrated circuit of Claim 11, wherein the external

2   integrated circuit is an egress backplane interface subsystem (EBISS), and the queues of the

3   external integrated circuit are first in, first out (FIFO) queues.

1   14.   (original) The integrated circuit of Claim 11, wherein the controller

2   circuitry is further configured to control operation of sending read cell pointers with

3   corresponding cell descriptors to the external integrated circuit, wherein each read cell pointer

4   points to a memory buffer that has been read and that is free to be reused.

1   15.   (original) The integrated circuit of Claim 11, wherein the operation of

2   storing free cell pointers further configures the controller circuitry to control operations of:

3   storing odd free cell pointers in an odd free list of the pointer RAM; and

4   storing even free cell pointers in an even free list of the pointer RAM.

1   16.   (original) The integrated circuit of Claim 11, wherein the operation of

2   temporarily storing free cell pointers further configures the controller circuitry to control

3   operations of:

4   storing odd free cell pointers in an odd free space of internal cache; and

5   storing even free cell pointers in an even free space of internal cache.

1   17.   (original) The integrated circuit of Claim 14, wherein the operation of

2   calculating free cell pointer counter values further configures the controller circuitry to control

3   operation of performing at least one of:

4   incrementing a free counter value to account for a cell pointer that has been sent

5   to the pointer RAM; and

6   decrementing a free counter value to account for a cell pointer that has been

7   received from the pointer RAM.

1   18.   (original) The integrated circuit of Claim 11, wherein the operation of

2   calculating free counter values further configures the controller circuitry to control operations of:

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3   determining that a free cell pointer counter value of the internal cache is above a

4   high threshold; and

5   writing a block of cell pointers in a burst to the pointer RAM.

1   19.   (original) The integrated circuit of Claim 11, wherein the operation of

2   calculating free counter values further configures the controller circuitry to control operations of:

3   determining that a free counter value of the internal cache is below a low

4   threshold; and

5   reading a block of free cell pointers in a burst from the pointer RAM.

1   20.   (original) The integrated circuit of Claim 11, wherein the operation of

2   calculating free cell pointer counter values further configures the controller circuitry to control

3   operations of:

4   determining that a free counter value of internal cache is above an overload

5   threshold; and

6   temporarily blocking storing of additional free cell pointers into internal cache.

1   21.   (currently amended) A computer-readable medium carrying one or more

2   sequences of one or more instructions for caching free cell pointers pointing to memory buffers

3   configured to store data traffic of network connections, the one or more sequences of one or

4   more instructions including instructions which, when executed by one or more processors, cause

5   the one or more processors to perform steps of:

6   storing free cell pointers into a pointer random access memory (RAM), wherein

7   each free cell pointer points to a memory buffer that is vacant and available for storing data

8   traffic;

9   temporarily storing at least one free cell pointer <u>from the pointer RAM</u> into

10   internal cache configured to assist in lowering a frequency of reads from and writes to the pointer

11   RAM;

12   receiving a request from an external integrated circuit for free cell pointers;

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13   sending <u>one or more</u> free cell pointers to <u>one or more</u> queues of the external

14   integrated circuit, <u>wherein the one or more free cell pointers comprise the at least one free cell</u>

15   <u>pointer temporarily stored in the internal cache,</u> wherein each free cell pointer <u>in the one or more</u>

16   <u>free cell pointers in</u> a̶ <u>the one or more queues</u> q̶u̶e̶u̶e̶ is configured to become a write cell pointer;

17   receiving at least one write cell pointer and a corresponding cell descriptor from

18   the external integrated circuit; and

19   calculating free counter values in order to keep track of the free cell pointers.

1   22.   (original) The computer-readable medium of Claim 21, wherein the

2   pointer random access memory (RAM) is external to controller circuitry configured to control

3   operations of the computer-readable medium.

1   23.   (original) The computer-readable medium of Claim 21, wherein the

2   external integrated circuit is an egress backplane interface subsystem (EBISS), and the queues of

3   the external integrated circuit are first in, first out (FIFO) queues.

1   24.   (original) The computer-readable medium of Claim 21, wherein the

2   instructions further cause the processor to perform a step of sending read cell pointers with

3   corresponding cell descriptors to the external integrated circuit, wherein each read cell pointer

4   points to a memory buffer that has been read and that is free to be reused.

1   25.   (original) The computer-readable medium of Claim 21, wherein the step

2   of storing free cell pointers further causes the processor to carry out steps of:

3   storing odd free cell pointers in an odd free list of the pointer RAM; and

4   storing even free cell pointers in an even free list of the pointer RAM.

1   26.   (original) The computer-readable medium of Claim 21, wherein the step

2   of temporarily storing free cell pointers further causes the processor to carry out steps of:

3   storing odd free cell pointers in an odd free space of internal cache; and

4   storing even free cell pointers in an even free space of internal cache.

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1   27.   (original) The computer-readable medium of Claim 24, wherein the step

2 of calculating free cell pointer counter values further causes the processor to carry out at least

3 one of:

4   incrementing a free cell pointer counter value to account for a cell pointer that has

5 been sent to the pointer RAM; and

6   decrementing a free counter value to account for a cell pointer that has been

7 received from the pointer RAM.

1   28.   (original) The computer-readable medium of Claim 21, wherein the step

2 of calculating free counter values further causes the processor to carry a step of determining that

3 a free counter value of the internal cache is above a high threshold, and wherein the instructions

4 further configure the processor to perform a step of writing a block of cell pointers in a burst to

5 the free pointer RAM.

1   29.   (original) The computer-readable medium of Claim 21, wherein the step

2 of calculating free counter values further causes the processor to carry out a step of determining

3 that a free counter value of the internal cache is below a low threshold, and wherein the

4 instructions further cause the processor to perform a step of reading a block of free cell pointers

5 in a burst from the pointer RAM.

1   30.   (original) The computer-readable medium of Claim 21, wherein the step

2 of calculating free counter values further causes the processor to carry a step of determining that

3 a free counter value of internal cache is above an overload threshold, and wherein the

4 instructions further cause the processor to perform a step of temporarily blocking storing of

5 additional free cell pointers into internal cache.

1   31.   (new) A method for storing data traffic of network connections, the

2 method comprising:

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3   storing free cell pointers into a pointer random access memory (RAM), wherein

4   each free cell pointer points to a memory location that is vacant and available for storing data

5   traffic;

6   temporarily storing at least one free cell pointer from the pointer RAM into cache;

7   receiving a request from an integrated circuit for one or more free cell pointers;

8   and

9   sending one or more free cell pointers to the integrated circuit, the one or more

10   free cell pointers including the at least one free cell pointer temporarily stored in the internal

11   cache, wherein each free cell pointer in the one or more free cell pointers is used to write data

12   traffic to a memory location associated with each free cell pointer.

1   32.   (new) The method of claim 31, wherein the RAM is external to the

2   integrated circuit.

1   33.   (new) The method of claim 31, further comprising returning free cell

2   pointers to the cache after data traffic has been written to memory locations associated with the

3   free cell pointers.

1   34.   (new) The method of claim 31, further comprising:

2   determining a cell including data traffic;

3   determining a free cell pointer; and

4   writing the data traffic to a memory location associated with the free cell pointer.

1   35.   (new) The method of claim 31, wherein the one or more free cell pointers

2   are stored in one or more queues in the integrated circuit.

1   36.   (new) The method of claim 31, wherein the cache is configured to assist

2   in lowering a frequency of reads from and writes to the pointer RAM

1   37.   (new) A system for storing data traffic of network connections, the

2   system comprising:

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3   a storage device comprising:

4   a pointer random access memory (RAM) configured to store free cell

5 pointers, wherein each free cell pointer points to a memory location that is vacant and available

6 for storing data traffic;

7   a cache configured to temporarily store at least one free cell pointer from

8 the pointer RAM;

9   an integrated circuit configured to store data traffic, the integrated circuit

10 configured to request one or more free cell pointers from the storage device and store data traffic

11 in memory locations,

12   wherein one or more free cell pointers from the storage device are sent to the

13 integrated circuit in response to the request, the one or more free cell pointers including the at

14 least one free cell pointer temporarily stored in the internal cache, wherein each of the one or

15 more free cell pointers is used to write data traffic to a memory location associated with each

16 free cell pointer.

1   38. (new) The system of claim 37, wherein the storage device is external

2 storage with respect to the integrated circuit.

1   39. (new) The system of claim 37, wherein the integrate circuit comprises one

2 or more queues configured to store the one or more free cell pointers.

1   40. (new) The system of claim 37, wherein the cache is configured to assist in

2 lowering a frequency of reads from and writes to the pointer RAM